IN THE CLAIMS:

Following is a complete listing of all claims in the application, with an indication of the status of each:

Claim 1 (Currently Amended). A vertical field effect transistor including

a semiconductor pillar conduction channel,

gate electrodes in trenches adjacent said semiconductor pillar,

a layer of insulator adjacent said gate electrodes and opposite said semiconductor pillar,

sidewalls adjacent said semiconductor pillar above said gate electrodes in said trenches,

insulator material in said trenches above said gate electrodes and ~~adjacent~~ **between** said sidewalls **and said layer of insulator**, said insulator material being selectively etchable relative to said sidewalls and said semiconductor pillar**, and**

at least one contact that is borderless to the gate electrodes.

Claim 2 (Currently Amended). A vertical transistor as recited in claim 1, further including isolation material adjacent said layer of insulator ~~and~~ surrounding said vertical transistor, said isolation material being selectively etchable relative to said layer of insulator.

Claim 3 (Currently Amended). A vertical transistor as recited in claim 2, ~~further including a contact~~ **wherein said at least one contact is** formed in an opening in said isolation material adjacent said insulator **material** to a conductive region at an end of said pillar.

Claim 4 (Currently Amended). A vertical transistor as recited in claim 1, ~~further including~~ **wherein said at least one contact includes**

a contact formed in an opening to an end of said pillar, and

a contact formed in an opening adjacent to and extending above said pillar to said gate structure and insulated from said pillar by an insulating sidewall on said pillar.

Claim 5 (Original). A vertical transistor as recited in claim 1, further including a spacer in said trench between said gate structure and a bottom of said trench.

Claim 6 (Currently Amended). An integrated circuit device including

isolation material surrounding transistor locations in a substrate,

vertical field effect transistors formed at said transistor locations and having a gate electrode structure formed in a trench,

a layer of insulator material in said trench between said isolation material and said gate electrode structure, said isolation material being selectively etchable relative to said layer of insulator, ~~and~~

a contact opening formed along an interface of said layer of insulator material and said isolation material**, and**

at least one contact that is borderless to the gate electrode structure.

Claim 7 (Original). A device as recited in claim 6, wherein said gate structure includes dual gate electrodes extending on opposite sides of a conduction channel.

Claim 8. (Currently Amended) A device as recited in claim 6, ~~**further including a contact**~~ **wherein said at least one contact is** formed in said contact opening in said isolation material adjacent said insulator **material** and extending to a conductive region extending below said pillar.

Claim 9. (Currently Amended). A device as recited in claim 6, ~~**further including**~~ **wherein said at least one contact includes**

a contact formed in an opening to an end of said pillar, and

a contact formed in an opening adjacent to and extending above said pillar to said

gate structure and insulated from said pillar by an insulating sidewall on said pillar.

Claim 10 (Currently Amended). A device as recited in claim ~~61~~ 6, further including a spacer in said trench between said gate structure and a bottom of said trench.

11 (Withdrawn). A method of making a semiconductor device including a field effect transistor, said method including steps of

forming a semiconductor pillar in a trench in a body of a first insulating material, said trench extending to a layer of semiconductor material,

forming a layer of a second insulating material on walls of said trench, and

etching a contact opening to said semiconductor material through said first insulating material selectively and adjacent to said second insulating material.

12 (Withdrawn). A method as recited in claim 11, including further steps of

forming a gate structure adjacent sides of said pillar,

forming layers and/or sidewalls of selectively etchable materials over said gate structure and said pillar, and

forming contact openings to an end of said pillar and said gate structure by selective etching of said layers at locations above and adjacent said pillar, respectively.

13 (Withdrawn). A method as recited in claim 11, including further steps of

defining a height of said pillar by thickness of a layer of sacrificial material.

14 (Withdrawn). A method as recited in claim 13, wherein said sacrificial material is germanium oxide.

15 (Withdrawn). A method as recited in claim 11, wherein said step of forming said pillar is performed by epitaxial semiconductor growth in a trench.

16 (Withdrawn). A method as recited in claim 11, wherein said step of forming said pillar is performed by etching of a layer of semiconductor material.

17 (Withdrawn). A method as recited in claim 11, including a further step of limiting a dimension of said pillar by a distance between isolation structures.

Claim 18 (Original). A transistor comprising

a substrate,

a first diffusion,

a second diffusion above said first diffusion,

a channel extending vertically between said first diffusion and said second diffusion,

a gate structure extending on at least one side of said channel, and

a contact to said first diffusion borderless to said gate structure.

Claim 19 (Original). A transistor as recited in claim 18, wherein said transistor is a vertical transistor and wherein said first diffusion is formed in said substrate and said second diffusion is formed on the channel.

Claim 20 (Previously Presented). A transistor as recited in claim 18, wherein said gate structure extends on two sides of said channel.

Claim 21 (Original). A transistor as recited in claim 19, wherein a contact to said gate extends above and on two sides of said second diffusion.

Claim 22 (Original). A transistor as recited in claim 19, further including separate contacts to separate portions of said gate structure on different sides of said channel.

Claim 23 (Original). A transistor as recited in claim 18, wherein said gate structure extends on at least three sides of said channel.

Claim 24 (Original). A transistor as recited in claim 18, further including a contact to said second diffusion borderless to said gate structure.

Claim 25 (Original). A transistor as recited in claim 18, wherein said transistor comprises a pillar of single crystal silicon having an edge.

Claim 26 (Original). A transistor as recited in claim 25, wherein said pillar comprises said first diffusion, said channel and said second diffusion, said gate structure extending adjacent said pillar.

Claim 27 (Original). A transistor as recited in claim 26, wherein said first diffusion extends into single crystal silicon beneath said pillar and extends below said gate structure for formation of a contact adjacent said gate structure.

Claim 28 (Original). A transistor as recited in claim 26, further comprising an insulator adjacent said gate structure, wherein said contact to said first diffusion comprises a conductive layer adjacent said insulator.

Claim 29 (Currently Amended). A transistor as recited in claim 26, wherein **a contact to** said gate structure is borderless to said second diffusion.

Claim 30 (Currently Amended). A transistor as recited in claim 26, wherein said contact to said second diffusion ~~**comprises**~~ **extends adjacent to** a spacer **which is** self-aligned to said edge.

Claim 31 (Original) A transistor as recited in claim 26, wherein said pillar extends above said gate structure.

Claim 32 (Original). A transistor as recited in claim 18, further comprising an isolation structure, wherein said transistor is self-aligned to said isolation structure.

Claim 33 (Currently Amended). A transistor as recited in claim 18, further comprising a contact between said first diffusion and another diffusion forming part of a second transistor, wherein said contact between said first diffusion and said another diffusion extends over **an area of** insulation between said first transistor and said second transistor.

Claim 34 (Original). A transistor as recited in claim 33, wherein said insulation comprises an etched and deposited isolation structure.

Claim 35 (Original). A transistor as recited in claim 34 wherein said substrate comprises SOI having buried oxide isolation and wherein said insulation comprises said buried oxide isolation.

Claim 36 (Original). A transistor as recited in claim 33, wherein said first transistor and said second transistor comprise an inverter and wherein said contact to said first diffusion is a contact to said inverter.

Claim 37 (Original). A transistor as recited in claim 18, wherein said gate structure comprises a continuous interior wall entirely surrounding said channel and spaced therefrom by a dielectric layer.

Claim 38 (Original). A transistor as recited in claim 18 wherein said gate structure is self-aligned to said channel.

Claim 39 (Original). A transistor as recited in claim 18 wherein said first diffusion comprises a dopant species provided separately from said second diffusion.

Claim 40 (Original). A transistor as recited in claim 18, wherein said channel is of sub-lithographic width.

Claim 41 (Original). A transistor as recited in claim 18, wherein said first diffusion includes

top and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a first diffusion contact formed in the opening.

Claim 42 (Original). A transistor as recited in claim 18, wherein said second diffusion includes

top and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a second diffusion contact formed in the opening.

Claim 43 (Original). A transistor as recited in claim 18, wherein said gate structure includes

top, bottom and side surfaces covered by a dielectric material,

a borderless opening at least through a portion of the dielectric material on said top surface, and

a gate contact formed in the opening.

Claim 44 (Original). A transistor as recited in claim 18, wherein said first diffusion, said second diffusion and said gate structure each include a borderless contact.

REMARKS

Applicant thanks the Examiner for indicating that claims 18-28, 31-39 and 41-44 are drawn to the allowable subject matter.

An amendment after final rejection was filed September 30, 2003, but was not entered in the case because it raised new issues. This amendment is similar to the September 30, 2003, but also addresses issues raised in the Advisory Action mailed October 10, 2003. In particular, claims 3 and 8 have been amended to recite "said insulator material" as suggested by the Examiner. In addition, claims 1 and 6 now specifically recite "at least one contact that is borderless..." Dependent claims 3, 4, 8, and 9 have accordingly been amended to address antecedent basis issues.

Claims 1-44 are currently pending in the application. By this amendment, claims 1-3, 7, 8, 10, 29-30, and 33 are amended in order to improve claim language. Support for the amendments is provided in at least Figure 24 and at pages 12-15 of the present specification. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

The Examiner has objected to claims 3, 8 and 10 for the following informalities: claim 3, line 4 the phrase "said insulator" is unclear whether it is being referred to the layer of insulator or the insulator material of claim 1; claim 8, line 4, the phrase "said insulator" is unclear whether it is being referred to "said insulator material" and claim 10 depends on nonexisting claim 61.

All these informalities were corrected by this amendment. Specifically, Claims 3 and 8 were amended to refer to "said layer of insulator" in order to describe the structure 910 shown in Figures 9 and up and comprises a layer of nitride surrounding the silicon pillar 710. Additionally, responding to the objection claim 10 was amended to properly depend from claim 6. Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

Claims 29, 30 and 40 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner states that the phrase "said gate structure is borderless to said second diffusion" is unclear because Figures 23C and 37C shows

the gate structure is borderless to the second diffusion. The Examiner also finds that it is unclear how the contact to said second diffusion comprises a spacer self-aligned to said edge described in claim 30. This rejection is respectfully traversed.

Responding to this rejection, as pointed out in the previous response the term "borderless" is used by Applicant to define a contact opening which can be produced by selective etching at an interface between two materials that can be selectively etched relative to each other. Silicon oxide and silicon nitride can be used as such a pair of materials and can be selectively etched relative to each other. This technique allows formation of an opening in one of the materials along its interface with the other. If etching is done in accordance with a mask feature of minimum lithographic size and overlapping the interface of the two materials, the opening will be smaller than can be resolved by a lithographic exposure and therefore it is "sub-lithographic" in dimensions. This novel technique allows formation in a convenient manner, extremely small contacts.

The Applicant is respectfully submits that the phrase "said gate structure is borderless to said second diffusion" in Claim 29 describes the structure created by the specific technique described above, which is also described through out the specification and particularly on page 14, lines 16-17.

The Examiner objected the Claim 30 for the reason that it is unclear how the "contact to said second diffusion comprises a spacer self-aligned to said edge". In order to correct claim language and avoid an ambiguity, Applicant amends Claim 30. Specifically, claim 30 now reads,

> " Claim 30. A transistor as recited in claim 26, wherein said contact to said second diffusion **~~comprises~~ extends adjacent to** a spacer **which is** self-aligned to said edge."

Additionally, preceding claim 29 was slightly amended to clarify this matter.

The term "sub-lithographic width" in Claim 40 objected to by the Examiner should be understood as smaller than features as obtained by lithographic exposure which is necessarily limited. By this term, Applicant emphasized that proposed borderless structure allows obtaining dimensions smaller than lithography allows. This matter is fully described on page 9, lines 21-23 and on page 3 lines 2-5.

The Examiner objected to the specification as failing to provide proper antecedent basis for the claimed subject matter for several limitations. This objection is respectfully traversed for the reason that the features identified by the Examiner have been described in the specification. Specifically, the phrase "said gate structure extends on at least three sides of said channel" in Claim 23, lines 2-3 is supported by page 12, line 19. Additionally, the phrase "said contact between said first diffusion and said another diffusion extends over insulation between said first transistor and said second transistor" in claim 33, line 2 is presented at page 14, lines 25-32, page 15, lines 1-9 and shown in Figure 23. The language of claim 38, line about "said structure is self-aligned to said channel" is described at page 12, line 7.

Claims 1-10 were rejected under 35 U.S.C. §102(e) as being clearly anticipated by Alavi et al. (U.S. Patent No. 6,392,271). This rejection is respectfully traversed based on the following discussion.

As it was earlier pointed out the present invention primarily focused on the transistor formation with use of a novel borderless technique, which allows creation of a contact without providing insulation over the structure by forming a contact opening in or along an existing insulator by selective etching. In order to emphasize this feature, by the present amendment claims 1 and 6 have been amended to include the recitation in regard to a borderless element. Specifically, Claim 1 as amended now recites:

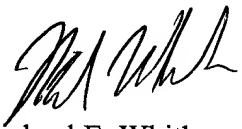
> "... insulator material in said trenches above said gate electrodes and ~~**adjacent**~~ **between** said sidewalls **and said layer of insulator**, said insulator material being selectively etchable relative to said sidewalls and said semiconductor pillar."
> (Emphasis added)

As it was discussed in the previous response, the reference to Alavi et al. does not teach a borderless structure and technique as is specifically required by claims 1 and 6. Alavi et al. shows a vertical MOS transistor, wherein the contact openings are formed by etching in accordance with lithographic patterning of an interlayer dielectric which is different from the Applicant's invention as claimed. It should be noted that Applicant's borderless approach allows contacts with the better dimensional characteristics then a lithography method could provide. Next, Applicant teaches a selective etching of insulator material surrounding gates, while Alavi et al.

proposes lithographically etch an ILD (inter-layer-dielectric) layer. Therefore, claim 1 as amended clearly distinguishes over the reference.

In view of the foregoing amendments and remarks, Applicant submits that all of the claims as amended are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456 of International Business Machines corporation (Burlington).

Respectfully submitted,



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